

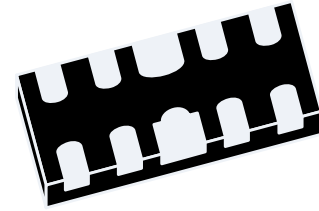
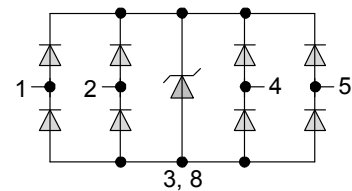
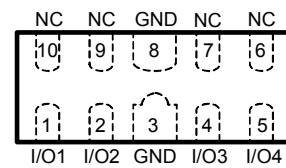
ESD5304D
**4-Lines, Uni-directional, Ultra-low Capacitance
Transient Voltage Suppressors**
<http://www.sh-willsemi.com>
Descriptions

The ESD5304D is an ultra-low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5304D incorporates four pairs of ultra- low capacitance steering diodes plus a TVS diode.

The ESD5304D may be used to provide ESD protection up to $\pm 20\text{kV}$ (contact discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20 μs) according to IEC61000-4-5.

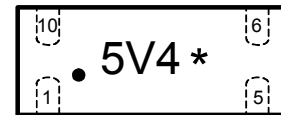
The ESD5304D is available in DFN2510-10L package. Standard products are Pb-free and Halogen-free.


DFN2510-10L (Bottom view)

Pin configuration (Top view)
Features

- Stand-off voltage: 5V max.
- Transient protection for each line according to IEC61000-4-2 (ESD): $\pm 20\text{kV}$ (contact discharge)
IEC61000-4-4 (EFT): 40A (5/50ns)
IEC61000-4-5 (surge): 4A (8/20 μs)
- Ultra-low capacitance: $C_J = 0.4\text{pF}$ typ.
- Ultra-low leakage current: $I_R < 1\text{nA}$ typ.
- Low clamping voltage: $V_{CL} = 19\text{V}$ typ. @ $I_{PP} = 16\text{A}$ (TLP)
- Solid-state silicon technology

Applications

- USB 2.0 and USB 3.0
- HDMI 1.3 and HDMI 1.4
- SATA and eSATA
- DVI
- IEEE 1394
- PCI Express
- Portable Electronics and Notebooks



5V4 = Device code
* = Month code (A~Z)

Marking
Order information

Device	Package	Shipping
ESD5304D-10/TR	DFN2510-10L	3000/Tape&Reel

Absolute maximum ratings

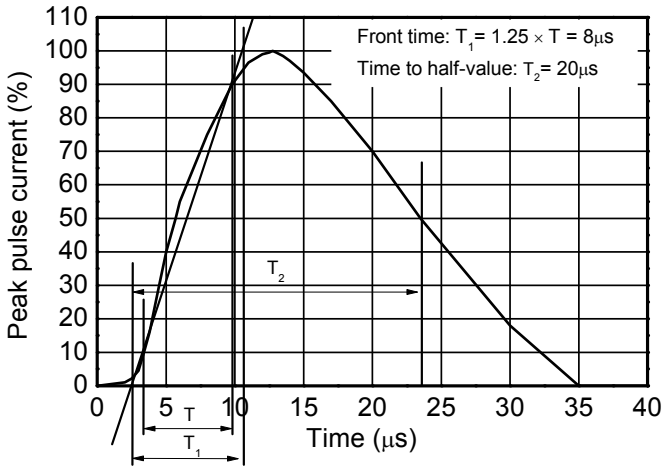
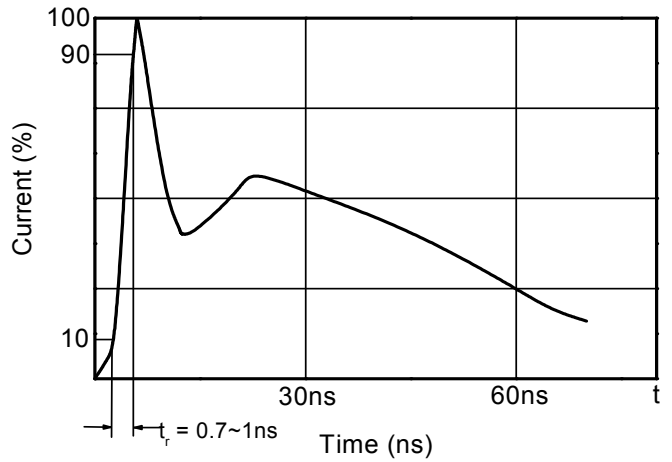
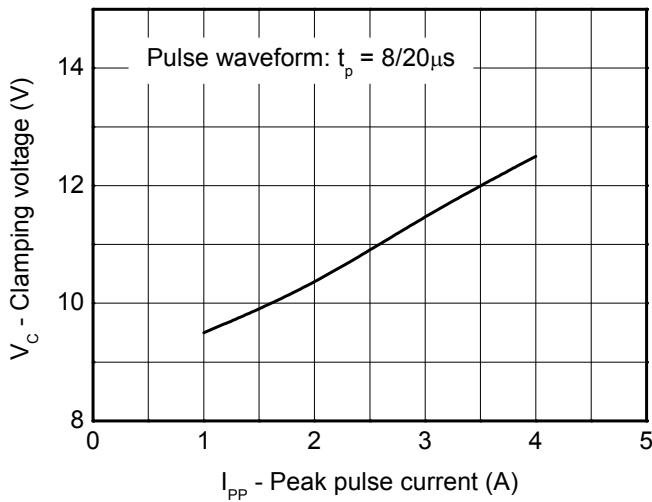
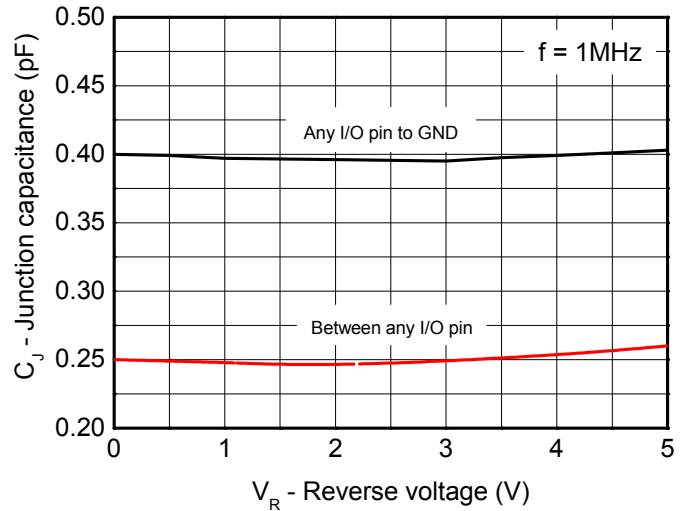
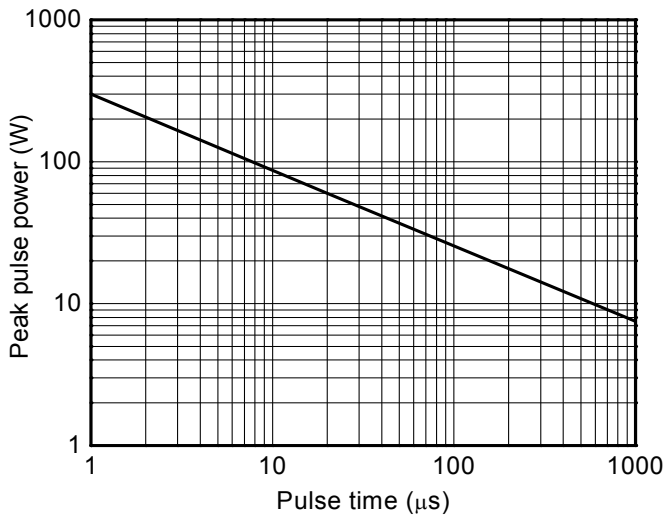
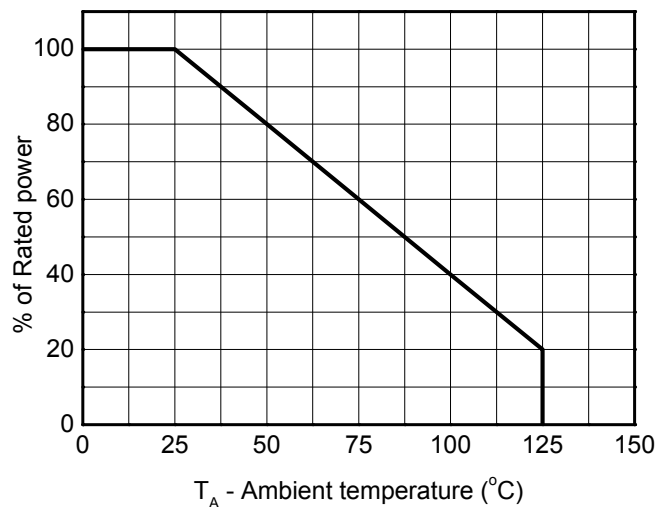
Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	60	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 20	kV
ESD according to IEC61000-4-2 contact discharge		± 20	
Operation junction temperature	T_J	125	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

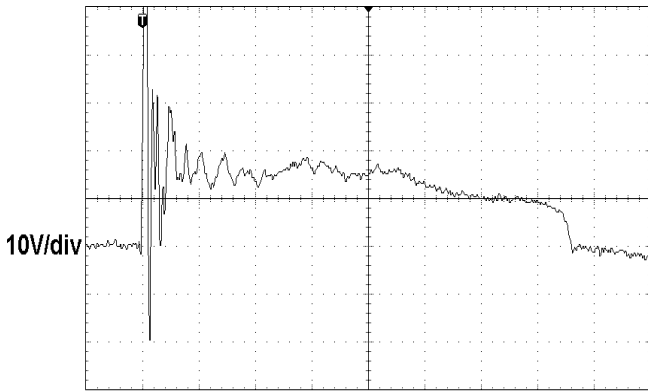
Electrical characteristics ($T_A = 25^{\circ}C$, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	$V_{RWM} = 5V$		<1	100	nA
Reverse breakdown voltage	V_{BR}	$I_T = 1mA$	7.0	8.0	9.0	V
Forward voltage	V_F	$I_T = 10mA$	0.6	0.9	1.2	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		19.0		V
Dynamic resistance ¹⁾	R_{DYN}			0.65		Ω
Clamping voltage ²⁾	V_{CL}	$I_{PP} = 1A, t_p = 8/20\mu s$			11	V
		$I_{PP} = 4A, t_p = 8/20\mu s$			15	V
Junction capacitance	C_J	$V_R = 0V, f = 1MHz$ Any I/O pin to GND		0.40	0.65	pF
		$V_R = 0V, f = 1MHz$ Between any I/O pin		0.25	0.40	pF

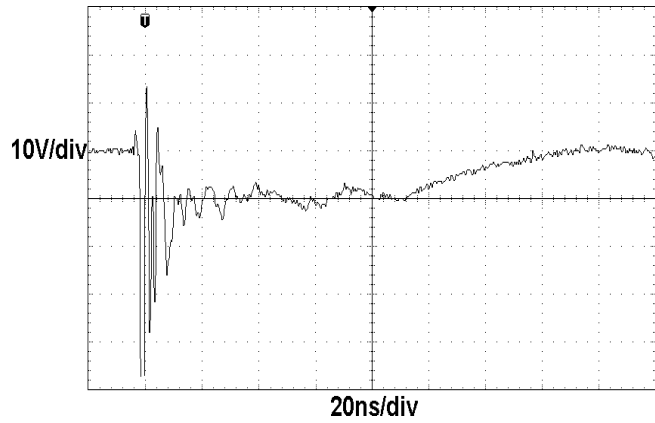
Notes:

- 1) TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) Non-repetitive current pulse, according to IEC61000-4-5.

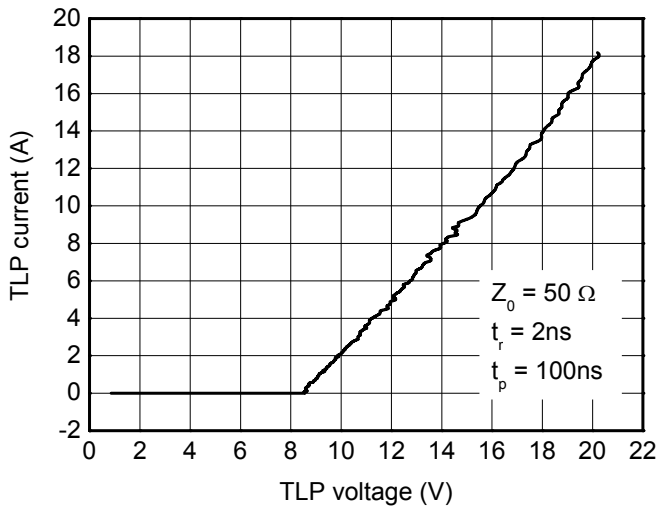
Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)

8/20 μs waveform per IEC61000-4-5

Contact discharge current waveform per IEC61000-4-2

Clamping voltage vs. Peak pulse current

Capacitance vs. Reverses voltage

Non-repetitive peak pulse power vs. Pulse time

Power derating vs. Ambient temperature

Typical characteristics ($T_A = 25^\circ\text{C}$, unless otherwise noted)


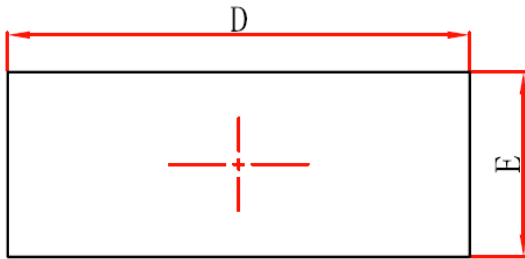
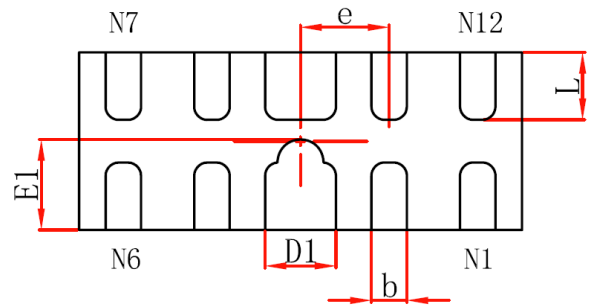
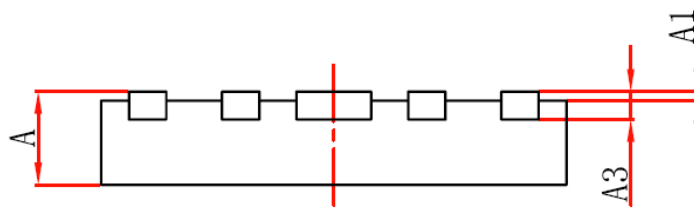
ESD clamping
 (+8kV contact discharge per IEC61000-4-2)



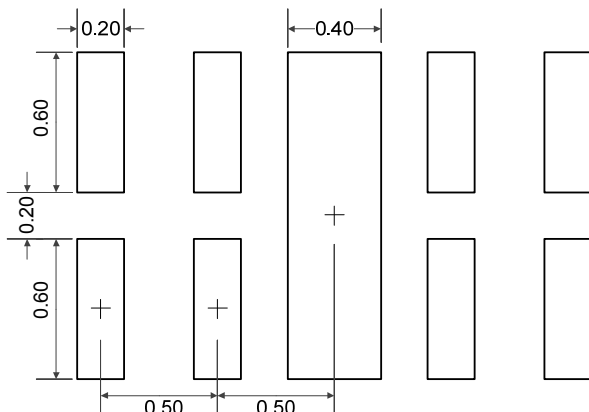
ESD clamping
 (-8kV contact discharge per IEC61000-4-2)



TLP Measurement

Package outline dimensions
DFN2510-10L

Top View

Bottom View

Side View

Symbol	Dimensions in millimeter		
	Min.	Typ.	Max.
A	0.550	0.600	0.650
A1	0.000	-	0.050
A3	0.150 Ref.		
D	2.424	2.500	2.576
E	0.924	1.000	1.076
D1	0.300	0.400	0.500
E1	0.410	0.510	0.610
b	0.150	0.200	0.250
e	0.500 Typ.		
L	0.304	0.380	0.456

Recommend Land Pattern (Unit: mm)

Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.