

WPMD2010

[Http://www.sh-willsemi.com](http://www.sh-willsemi.com)

Dual P-Channel, -20 V, -3.6A, Power MOSFET

Description

The WPMD2010 uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. This device is suitable for use in DC-DC conversion applications. Standard Product WPMD2010 is Pb-free.

Features

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ
-20 V	75mΩ@ -4.5V
	101mΩ@ -2.5V

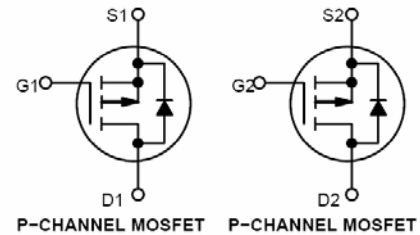
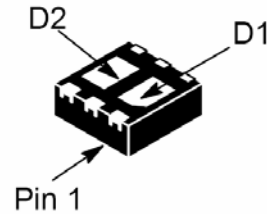
- Lower $R_{DS(on)}$ Solution in 2x2 mm Package
- 1.8 V $R_{DS(on)}$ Rating for Operation at Low Voltage Gate Drive Logic Level
- Low Profile (< 0.8 mm) for Easy Fit in Thin Environments
- Bidirectional Current Flow with Common Source Configuration
- DFN6 Package Provides Exposed Drain Pad for Excellent Thermal Conduction

Application

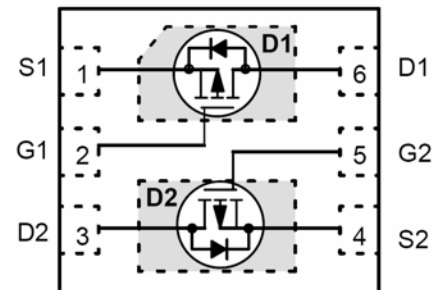
- Optimized for Battery and Load Management Applications in Portable Equipment
- Li-Ion Battery Charging and Protection Circuits
- High Power Management in Portable, Battery Powered Products
- High Side Load Switch

Order information

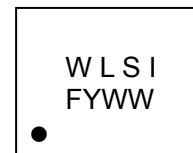
Part Number	Package	Shipping
WPMD2010-6/TR	DFN 6	3000Tape&Reel



PIN CONNECTIONS



MARKING DIAGRAM



F = Specific Device Code
YWW = Date Code

ABSOLUTE MAXIMUM RATINGS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted					
Parameter		Symbol	10 S	Steady State	Unit
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current ($T_J = 150\text{ }^\circ\text{C}$) ^a	$T_A = 25\text{ }^\circ\text{C}$	I_D	-3.6	-3.1	A
	$T_A = 70\text{ }^\circ\text{C}$		-2.9	-2.7	
Maximum Power Dissipation ^a	$T_A = 25\text{ }^\circ\text{C}$	P_D	2.0	1.5	W
	$T_A = 70\text{ }^\circ\text{C}$		1.3	1.0	
Continuous Drain Current ($T_J = 150\text{ }^\circ\text{C}$) ^b	$T_A = 25\text{ }^\circ\text{C}$	I_D	-2.3	-2.1	A
	$T_A = 70\text{ }^\circ\text{C}$		-1.8	-1.7	
Maximum Power Dissipation ^b	$T_A = 25\text{ }^\circ\text{C}$	P_D	0.8	0.7	W
	$T_A = 70\text{ }^\circ\text{C}$		0.5	0.4	
Pulsed Drain Current ^c		I_{DM}	-18		A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10\text{ s}$	$R_{\theta JA}$	50	62	$^\circ\text{C/W}$
	Steady State		65	82	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10\text{ s}$	$R_{\theta JA}$	125	150	
	Steady State		145	175	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	30	38	
Dual operation					
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10\text{ s}$	$R_{\theta JA}$	40	50	$^\circ\text{C/W}$
	Steady State		52	65	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10\text{ s}$	$R_{\theta JA}$	100	120	
	Steady State		116	140	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	25	30	

- Surface mounted on FR4 Board using 1 in sq pad size, 1oz Cu.
- Surface mounted on FR4 board using the minimum recommended pad size, 1oz Cu.
- Repetitive rating, pulse width limited by junction temperature, $t_p = 10\mu\text{s}$, Duty Cycle=1%

Electrical Characteristics

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		-0.1	μA	
			$T_J = 85^\circ\text{C}$		-1		
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			±100	nA	
ON CHARACTERISTICS							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-0.4	-0.6	-1.0	V	
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$		75	120	mΩ	
		$V_{GS} = -2.5\text{ V}, I_D = -2.5\text{ A}$		101	150		
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -3.1\text{ A}$		12		S	
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -10\text{ V}$	400	470	550	pF	
Output Capacitance	C_{OSS}		45	55	65		
Reverse Transfer Capacitance	C_{RSS}		40	50	60		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -2.7\text{ A}$	4	6	8	nC	
Threshold Gate Charge	$Q_{G(TH)}$		0.3	0.34	0.4		
Gate-to-Source Charge	Q_{GS}		0.5	0.75	1		
Gate-to-Drain Charge	Q_{GD}		1.0	1.2	1.5		
Gate Resistance	R_G			8.8			Ω
SWITCHING CHARACTERISTICS							
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, R_L = 3\ \Omega,$ $R_G = 6\ \Omega$	6	9	12	ns	
Rise Time	t_r		5	7	10		
Turn-Off Delay Time	$t_d(OFF)$		30	40	60		
Fall Time	t_f		5	7	10		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Recovery Voltage	VSD	$V_{GS} = 0\text{ V}, I_S = -1.6\text{ A}$	$T_J = 25^\circ\text{C}$	-0.7	-0.85	-1.5	V

Typical Performance Characteristics

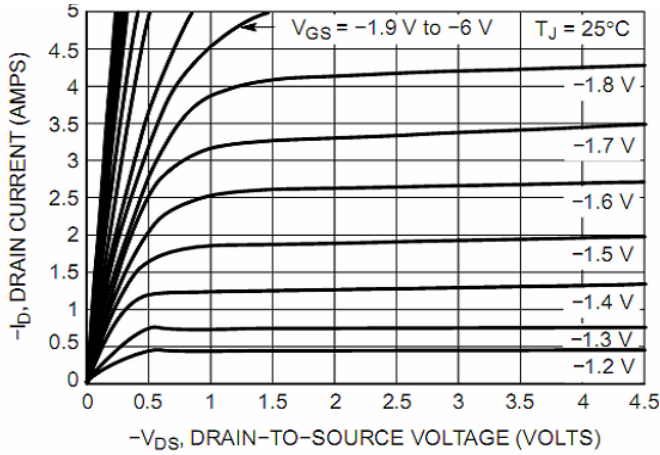


Figure 1. On-Region Characteristics

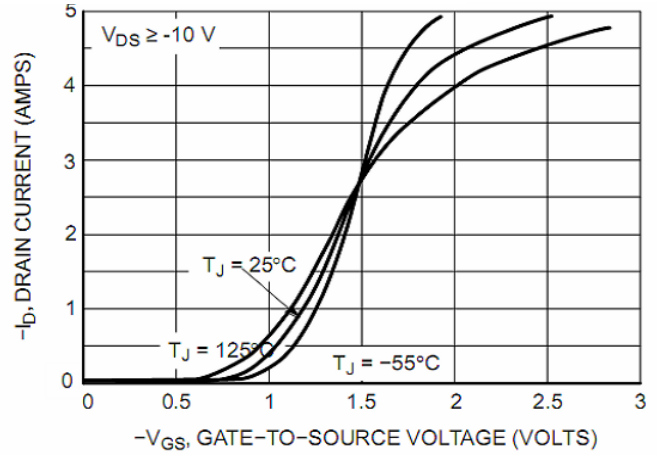


Figure 2. Transfer Characteristics

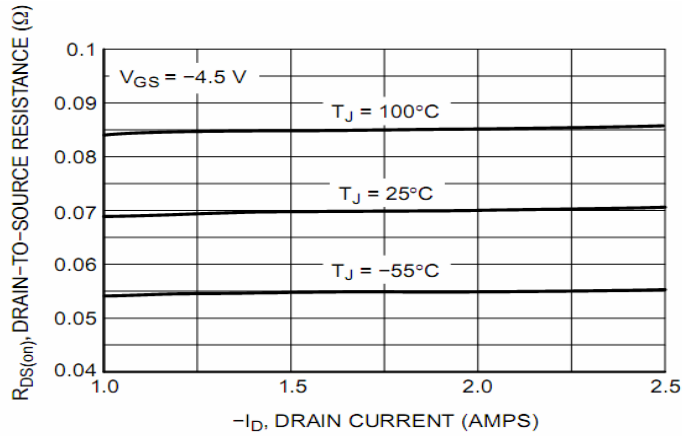


Figure 3. On-Resistance versus Drain Current

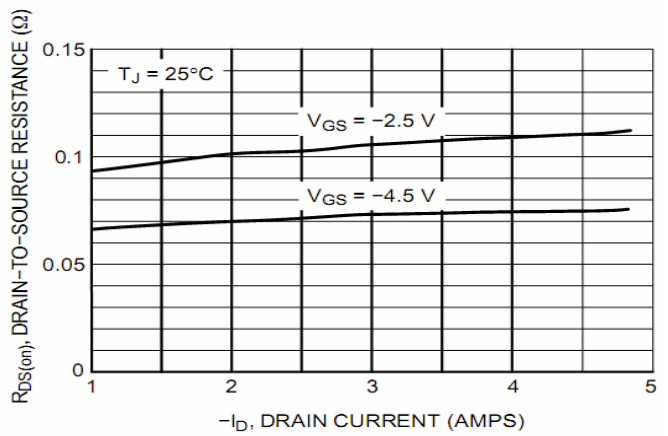


Figure 4. On-Resistance versus Drain Current and Gate Voltage

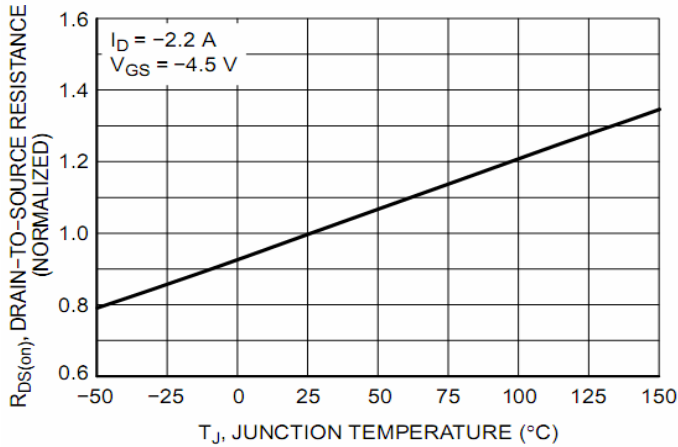


Figure 5. On-Resistance Variation with Temperature

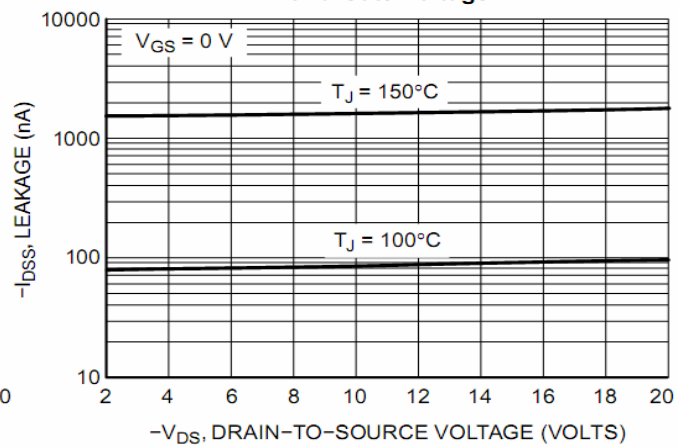


Figure 6. Drain-to-Source Leakage Current versus Voltage

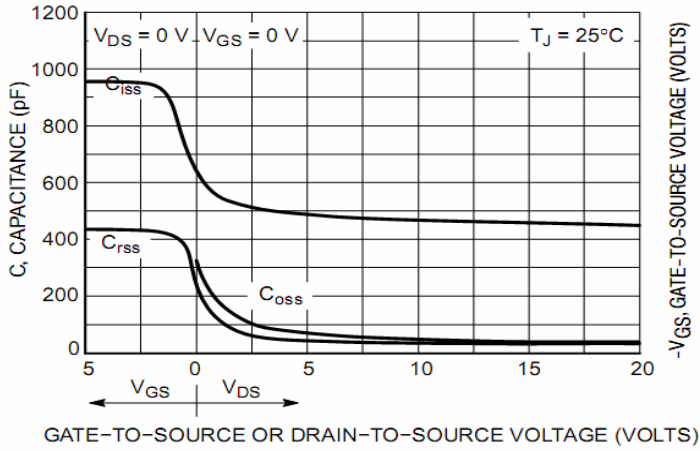


Figure 7. Capacitance Variation

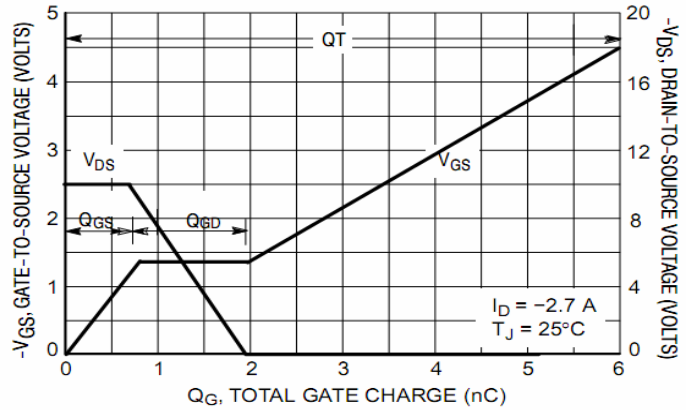


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

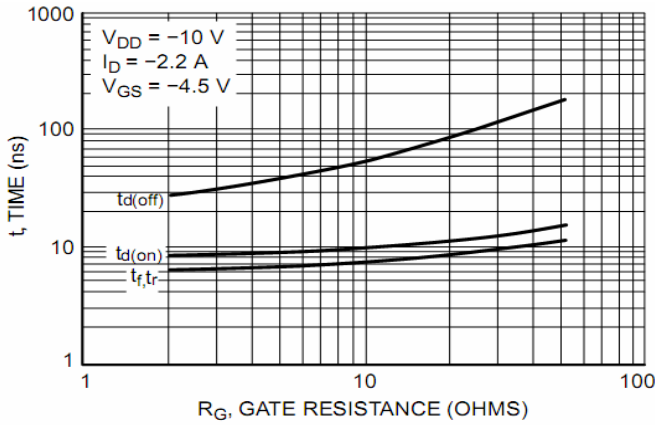


Figure 9. Resistive Switching Time Variation versus Gate Resistance

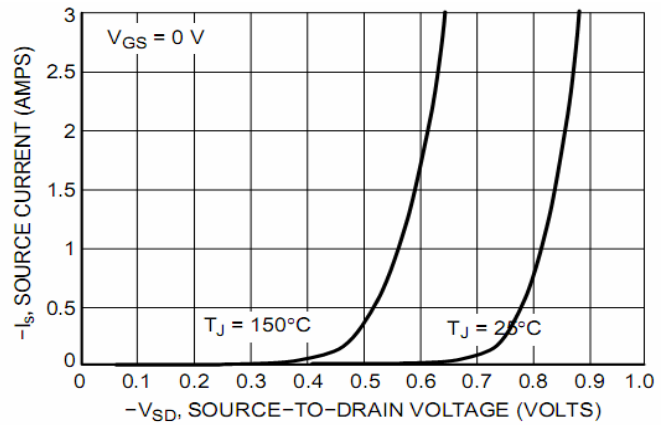


Figure 10. Diode Forward Voltage versus Current

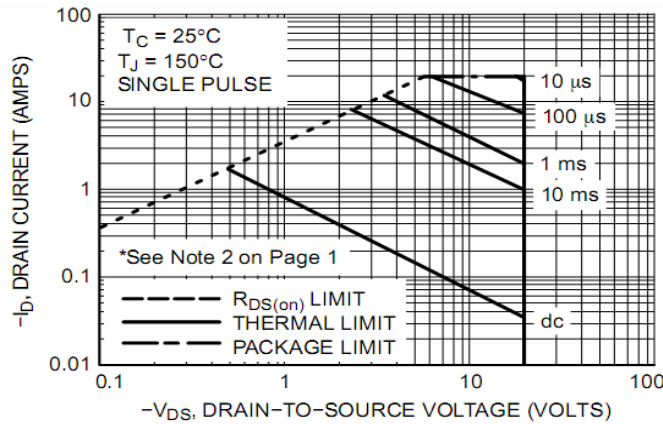


Figure 11. Maximum Rated Forward Biased Safe Operating Area

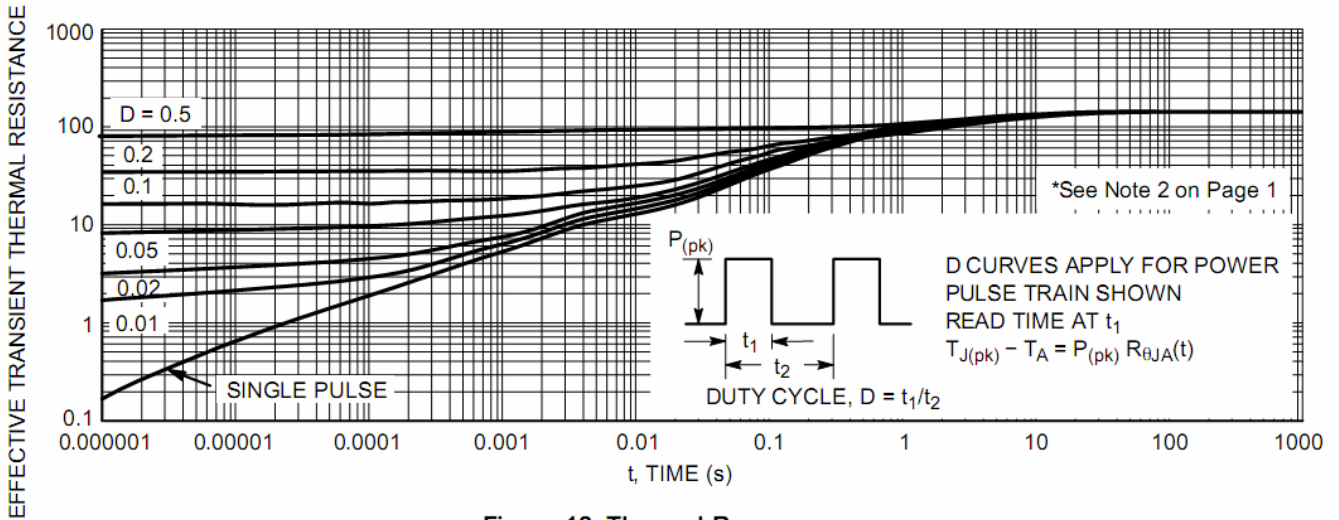
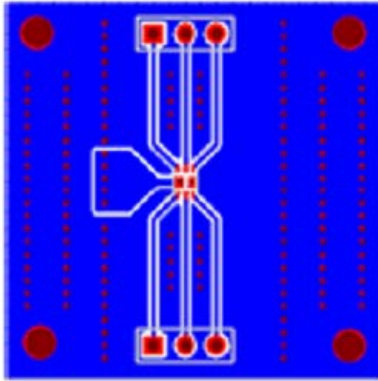


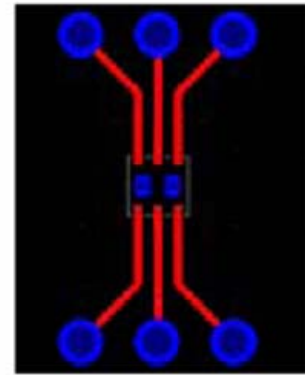
Figure 12. Thermal Response

Power Dissipation Characteristics

1. The package of WPMD2010 is DFN2x2-6L, surface mounted on FR4 Board using 1 in sq pad size, 2 oz Cu, R θ_{JA} is 82 °C/W, surface mounted on FR4 Board using minimum pad size, 2 oz Cu, R θ_{JA} is 175°C /W.
2. The power dissipation PD is based on $T_J (MAX) = 150^{\circ}C$, and the relation between T_J and Pd is $T_J = T_a + R_{\theta JA} * PD$, the maximum power dissipation is determined by R θ_{JA} .
3. The R θ_{JA} is the thermal impedance from junction to ambient; using larger PCB pad size can get smaller R θ_{JA} and result in larger maximum power dissipation.



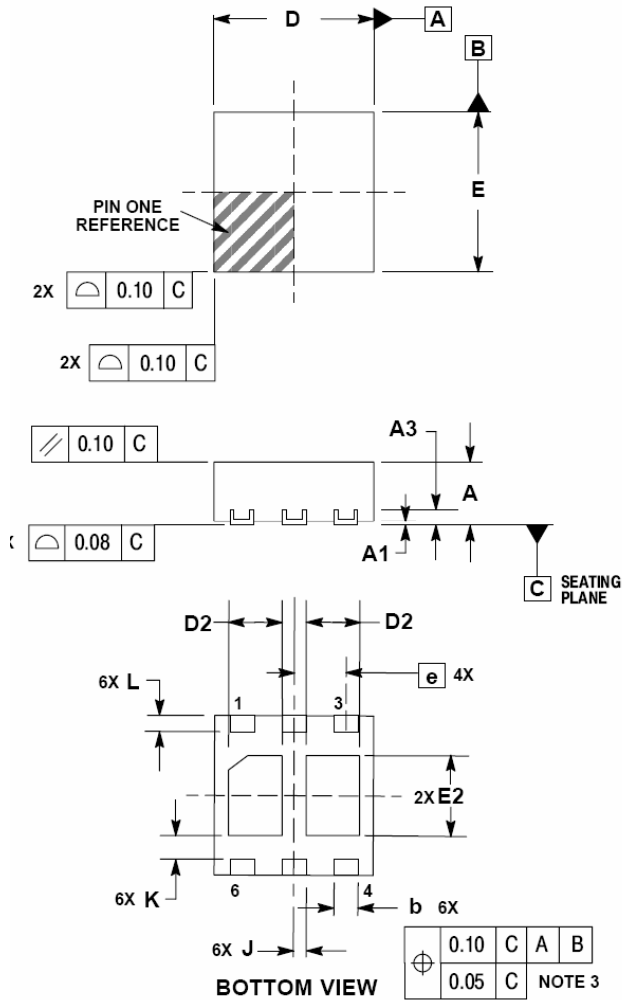
82 °C/W when mounted on
a 1 in² pad of 2 oz copper



175 °C/W when mounted on
a minimum pad of 2 oz copper

Packaging Information

DFN 6 Package Outline Dimension



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20mm FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
K	0.25 REF	
L	0.20	0.30
J	0.15 REF	

- STYLE 1:
- PIN 1. SOURCE1
 - GATE1
 - DRAIN2
 - SOURCE2
 - GATE2
 - DRAIN1

SOLDEMASK DEFINED MOUNTING FOOTPRINT*

